Remarks

I. Status of claims

Claims 3-13 and 21-33 were pending. Claims 13-20, 26, and 30 have been canceled without prejudice.

Claims 3 and 28 have been allowed.

Claims 25 and 27 have been rewritten in independent form in response to the Examiner's indication that such claims would be allowed.

II. Claim Rejections under 35 U.S.C. § 112, second paragraph

Claim 21 has been amended to address the Examiner's § 112, second paragraph, concerns.

III. Claim Rejections under 35 U.S.C. § 102(e)

The Examiner has rejected claim 13 under 35 U.S.C. § 102(e) over Jewell (US 6,243,508). Claim 13, however, has been canceled rendering the rejection moot.

IV. Claim Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected claims 4, 5, 7-9, 11, 12, 23, 26, and 29-31 under 35 U.S.C. § 103(a) over Jewell (US 6,243,508).

A. Claims 4, 5, 7-9, 12, 23, and 31

Independent claim 4 recites that the optical device substrate supports a solderable metallization pattern, the spacer substrate has a device bonding surface supporting a solderable metallization pattern, and a plurality of solder bumps are disposed between the metallization patterns of the optical device system and the optical lens system.

The Examiner has indicated that:

> Jewell et al. do not disclose the metallization patterns of the optical device system and the optical lens system. However, it would have been obvious to one of ordinary skill in the art to form the optoelectronic device of Jewell et al. comprising the optical device system and the optical lens system having the metallization patterns (i.e., bonding pads), because such structure is convention in the art for bonding the solder bump 148 to the optical device system or to the optical lens system.

In Jewell's device, the silicon-on-sapphire circuit layer 132 is the only element disposed between solder bump 148 and the optical wafer substrate 12. The circuit layer 132 corresponds to a layer of material that is formed by silicon-on-sapphire technology, which involves forming circuits from n- and p- channel transistors that consist of thin epitaxial islands of silicon grown on a sapphire substrate (i.e., optical wafer substrate 12). The Examiner has asserted that the circuit layer 132 corresponds to the spacer substrate recited in claim 4. In so doing, however, the Examiner is precluded from asserting that the silicon-on-sapphire circuit layer 132 corresponds to the claimed solderable metallization pattern supported by the device bonding surface of the spacer substrate. For this reason, the Examiner has asserted reflexively that it would have been obvious to modify Jewell's device to include such a metallization pattern. Contrary to the Examiner's assertion, however, it would not have been obvious to provide a metallization pattern on the silicon-on-sapphire circuit layer 132 that is disposed between the solder bump 148 and the optical wafer substrate 12 in Jewell's device because the silicon-on-sapphire circuit layer 132 already serves the function of a solderable metallization pattern. Thus, one of ordinary skill in the art at the time of the invention would not have been motivated to modify Jewell's device as proposed by the Examiner because such a modification would be redundant to the existing structure and, therefore, would not serve any useful purpose.

In addition, the Examiner has failed to establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103. Indeed, the Examiner's rejection amounts to an unsubstantiated assertion that it would have been obvious to modify Jewell's device to include an element recited in claim 4 "because such structure is convention in the art for bonding the solder bump 148 to the optical device system or to the optical lens system." The Examiner, however, has failed to provide "some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

art, to modify the [reference] ...," as required by MPEP § 706.02(j). For example, the Examiner has failed to explain why one of ordinary skill in the art at the time of the invention would have been motivated to provide the proposed "bonding structure" when the solder bump 148 in Jewell's device clearly is bonded to both the devices 26, 26' and the optical wafer substrate 12 without requiring any additional "bonding structure".

For at least these reasons, the Examiner's rejection of independent claim 4 under 35 U.S.C. § 103(a) over Jewell should be withdrawn.

Claims 5, 7-9, 12, 23, and 31 incorporate the features of independent claim 4 and, therefore, these claims are patentable for at least the same reasons.

B. Claims 11 and 29

Independent claim 11 recites that the optical device substrate supports a solderable metallization pattern, the optical lens system has a device bonding surface supporting a solderable metallization pattern, and a plurality of solder bumps are disposed between the metallization patterns of the optical device system and the optical lens system. Claim 11 is, therefore, patentable for at least the same reasons explained above in connection with independent claim 4. In particular, based on the Examiner's interpretation of Jewell's disclosure, Jewell's device does not include a solderable metallization pattern supported by a device bonding surface of an optical lens system, as recited in claim 11. As explained above, it would not have been obvious to provide a metallization pattern on optical wafer substrate 12 in addition to the silicon-on-sapphire circuit layer 132 that is disposed between the solder bump 148 and the optical wafer substrate 12 because the silicon-on-sapphire circuit layer 132 already serves the function of a solderable metallization pattern. Thus, one of ordinary skill in the art at the time of the invention would not have been motivated to modify Jewell's device as proposed by the Examiner because such a modification would be redundant to the existing structure and, therefore, would not serve any useful purpose.

In addition, contrary to the Examiner's assertion, Jewell fails to teach or suggest anything about selecting the characteristic dimension of a plurality of solder bumps as recited in claim 11. The Examiner has asserted that, based on figures 17, 19, lines 5-10 of column 16, and lines 43-46 of column 11, "it would have been obvious to one of ordinary skill in the art to form a plurality of solder bumps of Jewell et al. having a dimension that is selected

based upon a representative focal distance between the optical devices and the optical lenses in order to maximize the efficiency of receiving optoelectronic devices 26'." Jewell's teachings at lines 43-46 of column 11, relate to the embodiment shown in FIG. 4, and Jewell's teachings at lines 5-10 of column 16 relate to the different embodiment shown in FIG. 19.

The cited disclosure at lines 43-46 of column 11 does not teach or suggest that a characteristic dimension of any the solder bumps 148 is selected based upon a representative focal distance between the one or more optical devices and the one or more optical lenses. Indeed, the distance between the optical transducer 26 and the optical element 24 may be varied by selecting the thickness of any of the structural elements between the optical transducer 26 and the optical element 24. There is no teaching in Jewell that would have led one of ordinary skill in the art at the time of the invention to vary the distance between the optical transducer 26 and the optical element 24 by selecting a characteristic dimension of solder bumps 148 as opposed to selecting, for example, a characteristic dimension of the optical wafer substrate 24.

The cited disclosure at lines 5-10 of column 16 also does not teach or suggest that a characteristic dimension of any one the solder bumps 148 is selected based upon a representative focal distance between the one or more optical devices and the one or more optical lenses. Instead, this disclosure merely teaches that the distance between the transducer 26 and the optical element 184 is determined by the standoff heights of the solder bumps 148. Based on this disclosure, one skilled in the art at the time of the invention reasonably could have concluded that the standoff heights of the solder bumps 148 are taken as a given process parameter and the dimensions of the optical element 184 are selected to optimize performance. Indeed, the disclosure following lines 5-10 of column 16 relates only to the dimensions of optical element 184; there is no additional teaching relating to the standoff heights of solder bumps 148.

For at least these reasons, the Examiner's rejection of independent claim 11 under 35 U.S.C. § 103(a) over Jewell should be withdrawn.

Claim 29 incorporates the features of independent claim 11 and therefore is patentable for at least the same reasons.

C. Claims 26 and 30

Claims 26 and 30 have been canceled without prejudice, rendering the rejection of these claims moot.

V. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-1078.

Respectfully submitted,

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